IN THE SPECIFICATION

Presented below are specification changes showing the changes made.

On page 2, please replace lines 7-9 with the following rewritten paragraph:

REFERENCE TO RELATED APPLICATIONS

This application is a continuation of Application No. 10/428,724 filed May 1, 2003, which is a continuation of Application No. 10/117,875 filed April 5, 2002, U.S. Patent No. 6,597,196, which is a continuation of Application No. 09/482,149 filed January 12, 2000, U.S. Patent No. 6,462,578, which is a continuation of Application No. 08/909,928 filed August 12, 1997, U.S. Patent No. 6,051,991, which is a continuation of Application No. 08/534,500 filed September 27, 1995, abandoned, which is a continuation of Application No. 08/229,923 filed April 14, 1994, abandoned, which is a continuation-in-part of Application No. 08/101,197 filed August 3, 1993, U.S. Patent No. 5,457,410.

Please substitute the paragraph beginning on page 16, line 9, third full paragraph on page 16, with the following paragraph:

Figure 12A and Figure 12B show a block diagram of part of the multiple level routing network which encompasses Block Connectors to the MLA-3 Level with MLA Tabs for higher levels of routing networks.

Please substitute the paragraph beginning on page 40, line 1, first full paragraph on page 40, with the following paragraph:

Figure 12A and Figure 12B show a block diagram of part of the multiple level routing network which encompasses Block Connectors to the MLA-3 Level with MLA Tabs for higher levels of routing network (the I-Matrix is not shown). **Figure 12A and Figure 12B** show the interconnections of one set of Block Connectors and its corresponding higher levels of MLAs in the horizontal direction. There is also a corresponding perpendicular (e.g., vertical) group of routing network interconnecting the Block Connectors and the associated MLAs. This perpendicular group is not shown in **Figure 12A and Figure 12B** in order to avoid obscuring the present invention. Note that there is a corresponding copy of the routing network for each and every Block Connector and associated MLAs of the FPGA.

Please substitute the paragraph beginning on page 40, line 13, and ending on page on page 41, line 23 with the following paragraph:

Shown in **Figure 12A and Figure 12B** are thirty-two blocks 1201-1232. Each block is associated with a distinct and adjacent block along with two BC tabs (e.g., one horizontal and one vertical). Each of the Block Connectors 1201-1232 are couple to two selectable BC Tabs via a programmable switch. For example, block connector 1201 is coupled to selectable BC Tab 1233 through programmable switch 1234. The second group is not shown. A similar BC Tab interconnection scheme exists for block connectors 1217-1232 (both horizontally and vertically). For each BC Tab, there are bidirectional programmable drivers connectable to the MLA-1 routing lines. For example, BC Tab 1233 is selectively connectable to the MLA-1 routing line 1235 via

drivers 1236. These drivers can either be parallel to or perpendicular to the corresponding BC Tabs. In the currently preferred embodiment, the number of MLA-1 lines is half the number of Block Connectors, since for each Block Connector, there is a corresponding MLA-1 line plus another MLA-1 line which is perpendicular to the first MLA-1 line. Each MLA-1 line is connectable through programmable means to the corresponding Block Connector, MLA-2 and MLA-3 lines through their corresponding BC Tab. Note that the MLA-1 routing network together with I-Matrix lines and Block Connectors form the routing resources in a 2 x 2 Block area. This format enhances more complex logic function formation accessing and interconnecting the cells. Furthermore, the MLA-1 routing network, in addition to both I-Matrix lines and Block Connectors, become additional bi-directionally programmable access lines that can serve as access ports for the implementation of even more complex logic functions through connections by other MLA lines or Block Connectors from outside of the 2 x 2 Block area. By using programmable switches, the I-Matrix lines and block connectors which are not necessarily adjacent or congruent to the 2 x 2 Block areas can be selectively accessed. Hence, the total number of routing segments including I-Matrix lines, Block connectors, and MLA-1 lines grow geometrically when the growth is from a Block to 2 x 2 Blocks.

Please substitute the paragraph beginning on page 44, line 12, and ending on page on page 45, line 7 with the following paragraph:

In one embodiment, each Block Connector and BC Tab have extensions to the adjacent Blocks. For example, block 1201 is connectable to block 1202 via

programmable switch 1246. It should be noted that additional extensions for MLA lines can be implemented in order to extend the routing range without having to user higher level MLA lines. Multiple variations to the routing network shown in **Figure 12A and Figure 12B** are possible. For example, to increase routing resources and hence routability, the MLA-1 routing network can be replaced by making two copies of the MLA-2 routing network. On the other hand, if the objective is to minimize the routing area, one embodiment minimizes the amount of programming bits by replacing the MLA-1 routing network with a copy of the MLA-2 routing network. These kinds of variations can be applied to a mixture of other levels. Another embodiment is to off-set one or more of the MLA lines. For example, in **Figure 12A and Figure 12B**, the MLA-1 line 1247 is accessible by BC Tabs 1245, 1248, 1249, and 1250. The MLA-1 line 1247 can be shifted by one block to become accessible by BC Tabs 1248, 1251, 1250 and 1252 instead. All other MLA-1 lines can by thusly shifted. This can also be applied to other MLA level(s).

Please substitute the paragraph beginning on page 46, line 22, and ending on page on page 48, line 16 with the following paragraph:

Figure 16 shows one embodiment of a routing network for the MLA-4 layer and the mechanism whereby the MLA-4 lines are accessed. **Figure 16** shows four 8 x 8 Blocks 1621-1624 (for a total of 16 x 16 Blocks). Associated with the four 8 x 8 Blocks 1621-1624 are four horizontal and four vertical groups of MLA Tabs. In the currently preferred embodiment, the MLA-4 lines and MLA Tabs are 8-bits wide. Since each Block has eight corresponding Block Connectors, each MLA Tab is shown to be eight

lines wide where each of the lines corresponds to one of the 8 Block Connectors as shown earlier in **Figure 12A and Figure 12B**. In the currently preferred embodiment, there are four vertical and four horizontal MLA-4 lines, each of which is eight lines wide. Thus, the number of MLA-4 lines is one-fourth the number of MLA-3 lines. Each MLA-4 line is connectable through programmable means to the corresponding Block Connector, MLA-1, MLA-2 and MLA-3 lines. The desired connectivity is made through the corresponding MLA Tab and the BC Tabs. The MLA-4 routing network together with the I-Matrix lines, Block Connectors, MLA-1 routing network, MLA-2 routing network and MLA-3 routing network, form the routing resources in 16 x 16 Block area for more complex logic function formation accessing and interconnecting of the cells. In one embodiment, the MLA-4 routing network, in addition to both I-Matrix lines, Block Connectors, MLA-1 lines, and MLA-2 lines and MLA-3 lines become additional bi-directionally programmable access lines that can serve as access ports for the implementation of even more complex logic functions through connections by other MLA lines of Block Connectors from outside of 16 x 16 Block area through programmable means These other MLA lines or block connectors need not necessarily be adjacent or congruent to the 16 x 16 Block area. The total number of routing segments including I-Matrix lines, Block connectors, MLA-1 lines, MLA-2 lines, MLA-3 lines and MLA-4 lines in a 16 x 16 Block unit grows proportional to the increase in logic cells. The increase in size is geometrical when the growth is from a Block to 16 x 16 Blocks. Form each MLA Tab there is a corresponding MLA-4 lines connectable to the MLA Tab via a switch. For example, MLA Tab 1601 is connectable to MLA-4 line 1606 via switch

1607; and MLA-4 line 1608 via switch 1609. Likewise, MLA Tab 1610 is connectable through programmable means to all the corresponding MLA Tabs in all four corners through the vertical or the horizontal MLA-4 lines.